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FPGA-BASED FM MODULATOR WITH CARRIER DERIVED FROM A MODIFIED SINGLE OP-AMP JERK CIRCUIT

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ABSTRACT

In this paper, a digital oscillator derived from a modified single op-amp jerky type circuit as carrier of an FM modulator and its FPGA implementation is proposed. We studied the dynamics of the modified oscillator circuit jerky type and we derived from this study a stable oscillator so that its frequency can be controlled by one of its parameters. The regular oscillator designed is used to build a digital FM modulator and its FPGA-based implementation. The proposed digital FM modulator is made of a digital solver and a digital-to-analog converter. The post-synthesis of the modulator described with VHDL with fixed-point operations as per IEEE754 standards to be deployed on cyclone IV-EEP4CE115F29C7N of the board DE2-115 presents the following results: 10 688 logic elements, 96 registers, 35 embedded multipliers and an estimated power consumption of 152.83mW. In general, the proposed modulator design presents low area and power consummation. From the experimental results, it can be seen clearly and concluded that the model could be used as a digital modulator.

KEYWORDS: Stability analysis, Field Programmable Gate Array, Register transfer logic, Digital oscillator, FM, Jerk Circuit**.**

1 INTRODUCTION

Among the constraints observed in current audio broadcasting applications (private mobile radio and digital audio broadcasting terrestrial) are excellent clarity and even source stability during voice transmission. Modulation is a signal processing technique that involves switching or keying the amplitude, frequency, or phase of the carrier according to the information binary digits. There are three basic modulation schemes: amplitude shift keying (ASK), frequency shift keying (FSK), and phase shift keying (PSK). These schemes are, respectively, the binary equivalent of analog transmission's amplitude modulation (AM), frequency modulation (FM), and pulse modulation (PM) when used to transmit data signals. In a communication transmission chain, a modulator is a signal processor whose performance is critical for the overall SNR (Signal to Noise Ratio), EVM (Error Vector Magnitude) and BER (Bit error rate) specifications of the overall transmitter. For applications based on remote sensing, the modulator must present a minimal amplitude and phase imbalance so that the transmitter presents minimal EVM values. Most of audio broadcasting applications are implemented in a frequency modulation (FM) scheme. Many of techniques used to generate FM signals are based on some analog components while supporting broadcast audio standards. The analog FM modulation technique presents some difficulties due using a VCO (voltage-controlled oscillator). When a VCO is used in the analog modulation scheme, achieving good clarity and stabilizing the FM-modulated signal source is difficult. This difficulty is because the VCO is not linear over the desired frequency band. Consequently, there is a need for the digital FM technique. Digital FM modulation and demodulation techniques are widely used on mobile and FM devices. Almost all broadcasting systems need clear audio and voice signals to achieve excellent performance and vocal clarity. In most cases, the designers[1–6] have chosen to replace the VCO with an NCO (numerically controlled oscillator) to ensure linearity over the desired frequency band. Researchers have proposed several models of digital FM modulators. Among these models, some focus on the techniques for reducing the effects of noise distortion. The noise distortion mentioned here is caused by the quantization occurring during the resolution in bits at the input and at the output of the DDFS.[7] Others present an optimization through the use of hardware resources and low power consumption.[8-10] The DDFS architecture[11] is one of the first proposed DDFS. The required operations to build a DDFS are: generating a cosine waveform using a

phase accumulator and performing a phase-to-amplitude conversion. The techniques of designing a high-performance circuit for phase-to-amplitude conversion, quarter-wave symmetry ROM technique, and ROM compression techniques have been proposed by many researchers[12-15] to design DDFS. The ROM compression techniques present low-resolution bits and are not suitable as they maximize the error. The quarter-wave symmetry ROM technique presents a weak phase resolution. The ROM stated here is built using LUT or CORDIC. Ref.[16] showed that describing a function in VHDL optimizes some resources more than using LUT or CORDIC. To compute trigonometric and hyperbolic functions, the CORDIC algorithm is another method for computation. The rotation and vectoring modes are the two well-known leading basic CORDIC modes for the computation of different functions. The iterative sequence of additions/subtractions and shift operations are used to realize the two modes, which are rotations by a fixed rotation angle but with variable rotation direction. The CORDIC algorithm is a time-consuming computation task using more than 700 clock cycles[17, 18] for results computation. In binary representation, the precision of the evaluated results increases by 1 bit per iteration of the CORDIC computation. For example, the results will have a resolution of 16 bits with 16 CORDIC iterations. For example, the results will have a resolution of 16 bits with 16 CORDIC iterations. But this growth will start to saturate at about 24 bits. From the following two popular digital sine wave oscillators we can notice that the DDS need memory to store sample points and the memory capacity depends on the resolution of these sample points. The CORDIC algorithm is time-consuming, the number of iterations depends on the resolution of the sine output signal. Also, its lookup table is like in the DDS method. This implies that the latency increases with the resolution. These drawbacks of the above digital sine wave generation methods triggered us to investigate the use of the concept of generating oscillation using jerk circuit and the derived algorithm to implement in FPGA a digital sine wave. The derived algorithm from jerk circuit can permit the implementation of a digital sine wave generator. The main aim of this work includes: (a) studying a modify Jerky type circuit and coming out with the state equation of the oscillator, (b) deriving a stable oscillator and proposing the equivalent discrete equation of the stable oscillator state equation, (c) proposing a digital FM circuit-based digital oscillator. The rest of the paper is structured as follows: Section II presents the theoretical analysis of the modified op-amp jerk circuit and its state equations. The circuit design of the proposed FM digital modulator is described in detail in Section III. In Section IV, the FPGA-based implementation of the proposed FM digital modulator is presented, together with the simulation and experimental results obtained. Section V presents conclusions.

2. Modified jerk circuit oscillator and state equations

The schematic diagram depicted in Fig.1 is the Jerk circuit oscillator studied by[19], with its modified version shown in Fig. 2. The original circuit is a single Op-Amp-based Jerk chaotic oscillator. It is made up of one inductor with its internal resistance, two capacitors, one operational amplifier operating in its linear zone, and a JFET as the nonlinear element (NLE) of the oscillator. The proposed modified circuit is depicted in Fig. 2 below. It can be noticed that the nonlinear element of Fig. 1 is replaced by a pair of semiconductor diodes (D1, D2). By connecting two diodes in anti-parallel, as it can be observed in the circuit, a symmetrical characteristic[20] is obtained. When diodes are mounted so that the two terminals are shortened but with opposite polarities, the voltage across each diode is equal to the voltage across the resulting two terminal devices. The current flowing into the resulting two terminal devices is the sum of the current flowing through each diode.

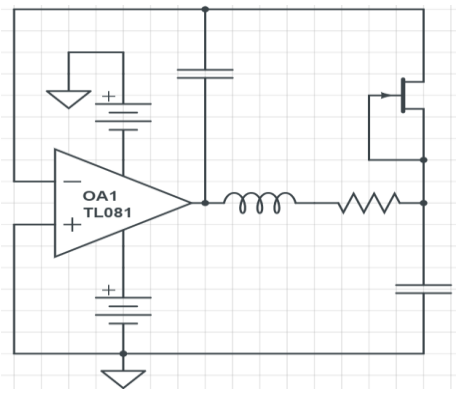

Fig. 1: A Single Op-Amp–Based Jerk Circuit Jerk.[17]

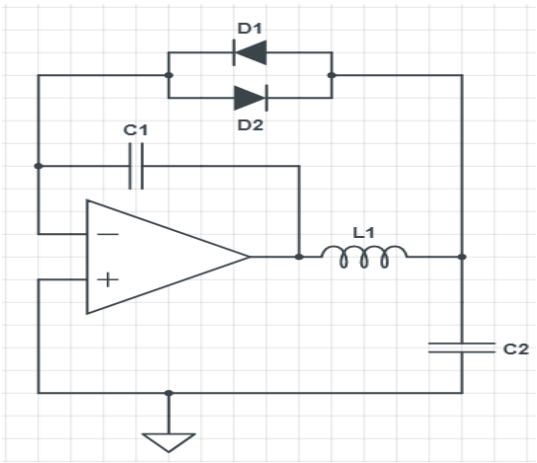

Fig. 2: Proposed Jerk Circuit with hyperbolic sine nonlinearity. The following values of electronic circuit components are used for analysis: a pair of signal diodes D1=D2=1N4148 ($\vartheta = 1.9, V_T = 26mV, I_s = 2.682nA$), the Op-amp is TL084CN.

2.1. The modified jerk circuit state equations

The proposed model of this paper is a purely mathematic model. For that reason, the following assumptions are valid: the inductor and capacitors are considered linear. The Op-amp is assumed to be operating in its linear working domain. The current-voltage characteristic of the semiconductor diodes' pair is obtained from the Shockley diode equation [21, 22]. To get it, let us consider I_{d1} as the current flowing into the diode D1, I_{d2} the current flowing into the diode D2 and I_d the current flowing into the resulting two terminal devices. That current-voltage characteristic is worth:

$$I_d = I_s\left[\exp\left(\frac{V_d}{\vartheta V_T}\right)-1\right]-I_s\left[\exp\left(\frac{-V_d}{\vartheta V_T}\right)-1\right]=2I_s\sinh\left(\frac{V_d}{\vartheta V_T}\right) \qquad (1)$$

where I_s is the saturation current of the junction; $V_T = k_b T/q$ is the thermal voltage with k_b the Boltzmann constant, T the absolute temperature in Kelvin, q the electron charge, and ϑ is the ideal factor $1 < \vartheta < 2$.

Denoting I as the current flowing through the inductor L_1 and V_{ci} $(i = 1,2)$ as the voltage across capacitor $C_i(i = 1, 2)$, the state equations of the circuit of Fig. 2 using the Kirchhoff law on the electric circuit are as follows:

$$\begin{cases} -C_1\dfrac{dV_{c1}}{dt} = 2I_s\sinh\left(\dfrac{V_d}{\vartheta V_T}\right) \\ C_2\dfrac{dV_{c2}}{dt} = I - 2I_s\sinh\left(\dfrac{V_d}{\vartheta V_T}\right) \\ L_1\dfrac{dI}{dt} = V_{C1} - V_{C2} \end{cases}. \qquad (2)$$

The Op-amp being ideal, $V_d = V_{C2}$. Following are the adopted change of variables and parameters:

$$t = \tau\sqrt{L_1C_1}, \gamma = \sqrt{\frac{L_1}{C_1}}, \varepsilon = 2I_s, \quad \sigma = \frac{C_1}{C_2}, \rho = \frac{1}{\vartheta V_T}, \qquad V_{C1} = x_1, V_{C2} = x_2, I = x_3 \qquad (3)$$

From equation (3), the normalized circuit equation of equation (2) is expressed by the following third-order differential equations:

$$\begin{cases} \dot{x}_1 = -\varepsilon\gamma\sinh(\rho x_2) \\ \dot{x}_2 = \sigma\gamma[x_3 - \varepsilon\sinh(\rho x_2)] \\ \dot{x}_3 = \dfrac{1}{\gamma}(x_1 - x_2) \end{cases}. \qquad (4)$$

Here the dots on the state variables denote their variation with respect to the dimensionless time. In the model system represented by equation (4), four parameters can be identified: two of these, namely $\varepsilon = 5.364 * 10^{-9}$, and $\rho = 20.243$ depend on intrinsic diode characteristics (the nonlinear element of circuit) and thus, are kept constant during all analysis. In contrast, the other two (γ and σ) depend on the linear elements of circuit. Therefore, the system's behavior will be studied in terms of the control parameters γ and σ, which are functions of the inductance and capacitances.

2.2 Equation points and analysis

The system is at rest at the equilibrium point, so the changes with time are nil. For that reason, the right-hand side of equation system (4) can be set equal to zero to calculate the system's fixed points.

$$\begin{cases} 0 = -\varepsilon\gamma \sinh(\rho x_2) \\ 0 = \sigma\gamma[x_3 - \varepsilon \sinh(\rho x_2)] \\ 0 = \dfrac{1}{\gamma}(x_1 - x_2) \end{cases} . \qquad (5)$$

Point $E_0(0,0,0)$ is the only solution of the system equation (5), and it is the only equilibrium point of the system. At the equilibrium point, the evaluation of the Jacobian matrix of system (5) is given by

$$J = \begin{bmatrix} 0 & -\varepsilon\gamma\rho & 0 \\ 0 & -\varepsilon\gamma\rho\sigma & \sigma\gamma \\ \dfrac{1}{\gamma} & -\dfrac{1}{\gamma} & 0 \end{bmatrix} . \qquad (6)$$

The stability of the equilibrium point $E_0(0,0,0)$ is determined by the sign of the real parts of the roots of the following characteristic equation ($det(J - \mu I_4) = 0$):

$$\mu^3 + \varepsilon\gamma\rho\sigma\mu^2 + \sigma\mu + \varepsilon\sigma\gamma\rho = 0. \qquad (7)$$

Using Routh-Hurwitz stability criterion, the condition for this equation to have all roots with negative real parts is given:

$$\sigma - 1 > 0 . \qquad (8)$$

From equation (8), it can be observed that the equilibrium $E_0(0,0,0)$ is stable if $\sigma > 1$ and unstable if $\sigma < 1$. Therefore, the necessity to study the Hopf bifurcation from the equilibrium point E_0 in the next paragraph.

Let $\mu = j\omega\ (\omega > 0)$ be a root of equation (7). Replacing $\mu = j\omega$ into equation (7) and grouping real and imaginary parts leads to

$$\sigma_c = 1,\ \ \omega_{Hopf}^2 = \sigma\ , \qquad (9a)$$

$$R_e\left(\frac{d\mu_{1,2}}{d\sigma}\Big|_{\sigma=\sigma_c}\right) = 4\varepsilon\rho^2 \neq 0\ . \qquad (9b)$$

Equation (9a) gives the critical value of the parameter σ for the system to oscillate. If the value of sigma is less than one ($\sigma < 1$), then system (4) will not oscillate. However, if the sigma value is above one ($\sigma > 1$), the system oscillates and displays a period-1limit cycle. Eq. (9b) shows that the transversality condition is always fulfilled.

From the above discussion, the system will generate self-excited oscillations for sigma values more significant than one.[23, 24] If the characteristic equation of a system admits an eigenvalue equal to -1 as the solution, then the system undergoes period-2-oscillations[23, 24], this means

$$\mu = -1 \qquad (10)$$

By substituting Eq. (10) into Eq. (7), we have

$$-1 + \varepsilon\gamma\rho\sigma - \sigma + \varepsilon\sigma\gamma\rho = 0. \qquad (11)$$

From Eq. (11), the parameter σ can be deduced:

$$\sigma = \frac{1}{2\varepsilon\gamma\rho - 1}\ . \qquad (12)$$

According to Eq. (3), σ is always positive. Now, system (4) cannot undergo period-2-oscillations because Eq. (12) imposes that σ should be negative, since $\varepsilon \approx 0$. Therefore, system (4) can only be set as a regular oscillator.

3. Proposed digital FM modulator circuit design

In the Frequency Modulation technique [24], the instantaneous frequency of the carrier signal varies linearly with the baseband-modulated message signal $m(t)$ as follows:

$$S_{FM}(t) = A_c COS\left[2\pi f_c t + 2\pi k_f \int_0^t m(t)dt\right]. \qquad (13)$$

Here, A_c is the carrier's amplitude, f_c is the carrier's frequency, and k_f is the frequency deviation constant. From this, the instantaneous frequency of the modulated frequency is given by:

$$f_i = f_c + k_f m(t). \quad (14)$$

Eq. (13) and Eq. (14) show that an FM modulator is a regular oscillator whose frequency is controlled by a signal message. Section 1 shows that system (4) is a regular oscillator. It has also been demonstrated that if $\sigma > 1$, the system will behave as a stable oscillator and oscillate, displaying a period-1 limit cycle, with the following frequency expression:

$$\omega_0^2 = \sigma \quad (15)$$

From Eq. (15), it can be noted that the parameter σ can control the frequency of system (4), or a factor depending on the inductance can be introduced to multiply sigma, then fix the value of sigma and vary the frequency of the oscillator thanks to the introduced factor. It implies that by varying the value of the inductance, the frequency of system (4) can be varied. Using system (4) and giving a fixed value to σ, the oscillator's frequency will depend on the inductance. Implementing the proposed oscillator using discrete components may be complex. For, the values of the capacitors and inductance to be chosen to cover the desired range of frequency may force the parasitic capacitors and inductors of the Op-Amp to be active and then change the dynamic of the proposed model. Nevertheless, system (4) can be implemented as a digital FM modulator using FPGA with a few modifications.

3. 1 Frequency-controlled oscillator circuit design

Theoretically, it was shown that system (4) could operate as a frequency-controlled oscillator. With the following few modifications on system (4): the parameter value $\boldsymbol{\varepsilon}$ is negligible compared to $\boldsymbol{\gamma}$, so it can be considered that that $\boldsymbol{\varepsilon\gamma} \approx \boldsymbol{\varepsilon}$ and replacing $\frac{1}{\gamma}$ by $\boldsymbol{\gamma}$, this enables obtaining system (16), a pure mathematical model presenting the same dynamic as system (4)

$$\begin{cases} \dot{x}_1 = -\varepsilon \sinh(\rho x_2) \\ \dot{x}_2 = \sigma[\gamma x_3 - \varepsilon \sinh(\rho x_2)]. \\ \dot{x}_3 = \gamma(x_1 - x_2) \end{cases} \quad (16)$$

The equilibrium analysis of system (16) shows that $E_0^*(0,0,0)$ is its equilibrium point. Eq. (17) is the Jacobian matrix around that equilibrium point E_0^*. Eq. (18) is the characteristic equation, and Eq. (19) depicts the Hopf bifurcation criterion.

$$M_j = \begin{bmatrix} 0 & -\varepsilon\rho & 0 \\ 0 & -\varepsilon\rho\sigma & \sigma\gamma \\ \gamma & -\gamma & 0 \end{bmatrix}, \quad (17)$$

$$\mu^3 + \varepsilon\rho\sigma\mu^2 + \sigma\gamma^2\mu + \varepsilon\rho\sigma\gamma^2 = 0\,, \quad (18)$$

$$\sigma - 1 > 0\,, \quad \omega_0 = \gamma\sqrt{\sigma} \quad , \quad and \quad \sigma_c = 1. \quad (19)$$

Eq. (19) shows that system (16) is a regular oscillator whose the frequency can be controlled by the parameter γ with the value of σ chosen greater than 1. Fig. 2 presents the state variable x_2 in the time domain and the phase portrait (x_2, x_3) with $\sigma = 1$ where γ has two different values.

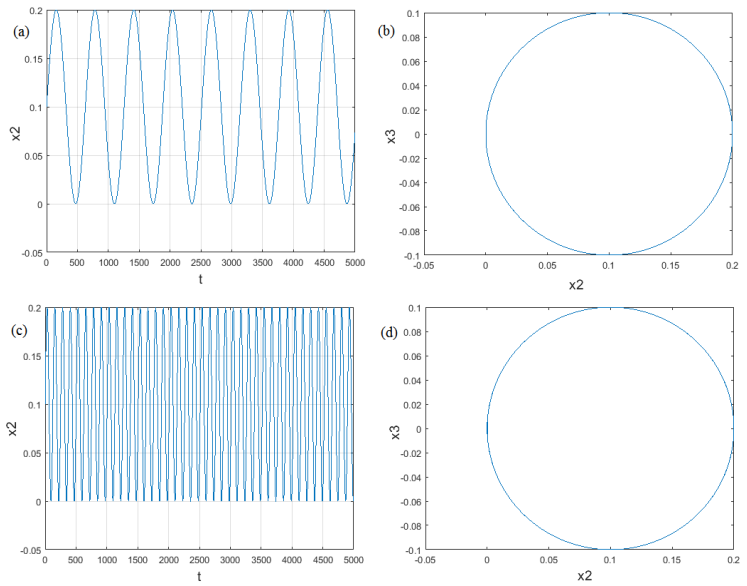

Fig. 2: Time evolution of x_2 and phase portrait of (x_2, x_3) of system (17): the graphs (a) and (b) are drawn with $\gamma = 0.01$; the graphs (c) and (d) are drawn with $\gamma = 0.05$.

Fig. 2 shows that system (16) behaves as a regular oscillator of period-1 limit cycle, and its frequency can be controlled by the parameters γ and σ. Therefore the system represented by (16) is a frequency-controlled oscillator when $\sigma = 1$. Since ε is too small, it can still be stated that $\varepsilon \sinh(\rho x_2) \approx \varepsilon\rho$. From this approximation, system (16) equals system (20). The time evolutions of system (16) and system (20) shown on Figure 3 confirm this approximation.

$$\begin{cases} \dot{x}_1 = -\varepsilon\rho x_2 \\ \dot{x}_2 = \sigma[\gamma x_3 - \varepsilon\rho x_2] \\ \dot{x}_3 = \gamma(x_1 - x_2) \end{cases}. \quad (20)$$

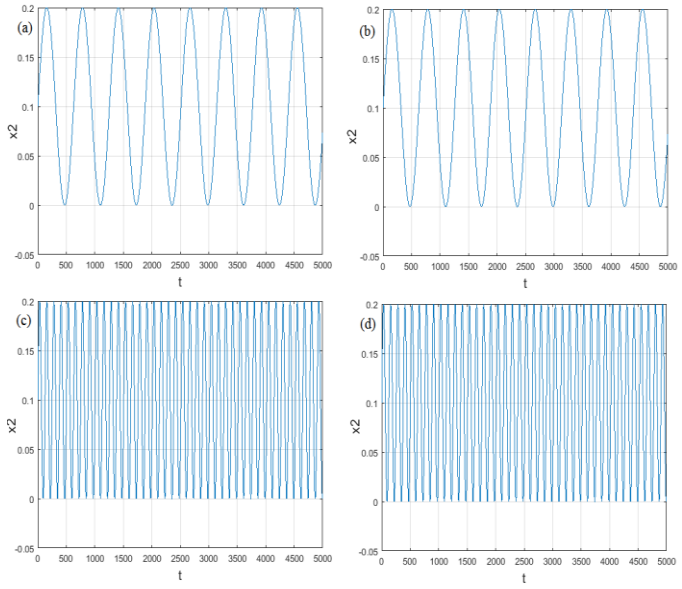

Fig. 3: Time evolution of the state variable x_2 of system (16) and system (20): (a) system (16) with $\gamma = 0.01$; (b) system (20) with $\gamma = 0.01$; (c) system (16) with $\gamma = 0.05$; (d) system (20) with $\gamma = 0.05$.

Because systems (16) and (20) present the same dynamic, we will adopt system (20) to design the digital FM circuit since it does not have any term to be linearized. In contrast, system (16) has the term $\sinh(\rho x_2)$ to linearize, which will lead to the consumption of more hardware resources.

A. Digital FM Circuit Design

3. 2 Digital FM circuit design

The block diagram presented in Fig. 4 is the proposed digital FM circuit to mimic the system's dynamic described by (20). The circuit is made of two blocks: a digital solver and a DAC. The digital solver used here is a circuit capable of implementing a numerical method to solve the dynamical system of equations (20). In section 2.1 above, it was shown that if the parameter $\sigma = 1$, system (20) is a regular oscillator with a frequency depending on the parameter γ, which means the frequency of the digital signal x_2 depends on the digital input message. The amplitude of the digital input message here is tailored to vary between 0.02 and 0.06 in the floating point format. The DAC circuit converts digital signal into the standard analog FM signal.

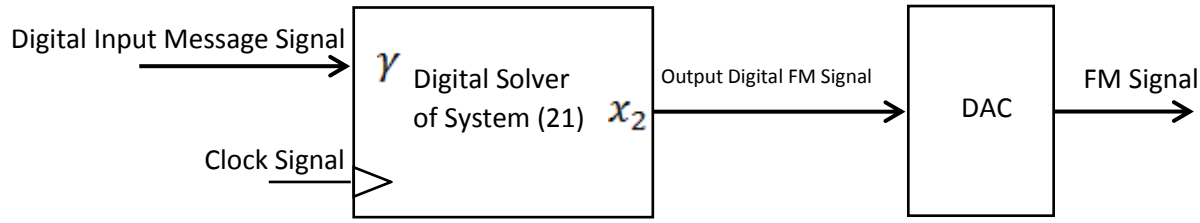

Fig. 4: Proposed Digital FM circuit Design using system (20) field programmable gate array-based implementation of the proposed digital QPSK modulator.

4. Field Programmable gate array based implementation of the proposed digital FM modulator

FPGAs are adequate devices for implementing digital FM modulators, such as the one in Fig. 4, based on the mathematical system (20) [16, 25-27]. In the present case, a choice has to be made about which numerical method will be suitable to solve the dynamic system (20). Doing this is equivalent to writing the dynamic system in the very high-speed integrated circuit hardware description language (VHDL). The Forward Euler method is considered for solving system (20) to generate the carrier frequency with a stable value, so $\sigma = 1$. Thus, the following discrete system of equations is obtained:

$$\begin{cases} x_{1n+1} = x_{1n} + h(-\varepsilon\rho x_{2n}) \\ x_{2n+1} = x_{2n} + h(\gamma x_{3n} - \varepsilon\rho x_{2n}) \\ x_{3n+1} = x_{3n} + h(\gamma(x_{1n} - x_{2n})) \end{cases} \qquad (21)$$

Before using VHDL to describe it, let us first calculate the convergence of the discrete system. This requires rewriting equation (21) in the following matrix:

$$\begin{pmatrix} x_1 \\ x_2 \\ x_3 \end{pmatrix}_{n+1} = \begin{pmatrix} 1 & -h\varepsilon\rho & 0 \\ 0 & 1 - h\varepsilon\rho & h\gamma \\ h\gamma & -h\gamma & 1 \end{pmatrix} \begin{pmatrix} x_1 \\ x_2 \\ x_2 \end{pmatrix}_n = A \begin{pmatrix} x_1 \\ x_2 \\ x_3 \end{pmatrix}_n = A^{n+1} \begin{pmatrix} x_1 \\ x_2 \\ x_3 \end{pmatrix}_0 \qquad (22)$$

The stability of equation (22) depends on the matrix A, whose eigenvalues must be determined by solving the equation $\det(A - \mu I) = 0$. After calculation, we have the following:

$$(1-\mu)^3 + (1-\mu)^2[(h\gamma)^2 - h\varepsilon\rho] + h\varepsilon\rho(h\gamma)^2 = 0. \qquad (23)$$

Taking into consideration that $\varepsilon \approx 0$, equation (23) can be written as

$$(1-\mu)^2[1 - \mu + (h\gamma)^2] = 0. \qquad (24)$$

From equation (24), we can see $\mu = \{1, 1 + (h\gamma)^2\}$. Because the eigenvalues have positive reel parts, matrix A is not stable, and system (22) cannot converge. Thus, the system cannot

be implemented using equation (22). Another simple and popular ODE solver is the fourth-order Rung-Kutta method. The Rung-Kutta recurrent algorithm is weakly suitable for hardware implementation. Therefore, in the present paper, the parallelized classical fourth-order Rung-Kutta method will be considered for constructing an efficient ODE solver with pipeline architecture as proposed by P. Fedoseev et al. [28]. Considering that $\varepsilon \approx 0$ equation (20) can now be reading as follow:

$$\begin{cases} \dot{x}_2 = \gamma x_3 \\ \dot{x}_3 = -\gamma x_2 \end{cases} . \qquad (25)$$

Equation (25) has as eigenvalues $\gamma = \mp i\sqrt{\gamma}$. From this eigenvalues, we can say that equation (25) admits stable solutions. Let us now start by applying the expansion of the Rung-Kutta recurrent formulas on equation (25):

$$x_{2n+1} = x_{2n} + \frac{h}{6}[6\gamma x_{3n} - 3\gamma^2 h^2 x_{2n} - \gamma^3 h^3 x_{3n} + \gamma^4 \frac{h^3}{4} x_{4n}]$$

$$x_{3n+1} = x_{3n} + \frac{h}{6}\left[-6\gamma x_{2n} - 3\gamma^2 h^2 x_{3n} + \gamma^3 h^3 x_{2n} + \gamma^4 \frac{h^3}{4} x_{3n}\right].$$

Reducing the numbers of mathematical operations by simplifications yields the following:

$$\begin{cases} x_{2n+1} = a_1 x_{2n} + a_2 x_{3n} \\ x_{3n+1} = -a_2 x_{2n} + a_1 x_{3n} \end{cases} \qquad (26)$$

with $a_1 = \left(1 - \frac{(\gamma h)^2}{2} + \frac{(\gamma h)^4}{24}\right), a_2 = \left(h\gamma - \frac{(\gamma h)^3}{6}\right)$

System (26) into the matrix form becomes:

$$\begin{pmatrix} x_2 \\ x_3 \end{pmatrix}_n = B^{n+1} \begin{pmatrix} x_1 \\ x_2 \end{pmatrix}_0 \qquad (27)$$

With $B = \begin{pmatrix} a_1 & a_2 \\ -a_2 & a_1 \end{pmatrix}$

The stability of equation (27) depends on the matrix B. Its eigenvalues are determined by solving the equation $\det(B - \mu I) = 0$, whose expansion gives

$$(a_1 - \mu)^2 + a_2^2 = 0 \qquad (28)$$

From equation (28), the eigenvalues can be written as follow;

$$\mu = a_1 \mp i a_2 \qquad (29)$$

Let define $f(\gamma h) = a_1 = 1 - \frac{(\gamma h)^2}{2} + \frac{(\gamma h)^4}{24}$, drawing the functions $f(\gamma h)$ will enable us to understand the variation of the eigenvalues.

Fig. 5 depicts the function $f(\gamma h)$ and we can notice that the expression a_1 is nil for two values. By choosing γh so that the function $f(\gamma h)$ is zero, the eigenvalues in equation (29) are complex numbers with the real part equal to zero means that the solutions of equation (27) are pure sinusoidal functions.

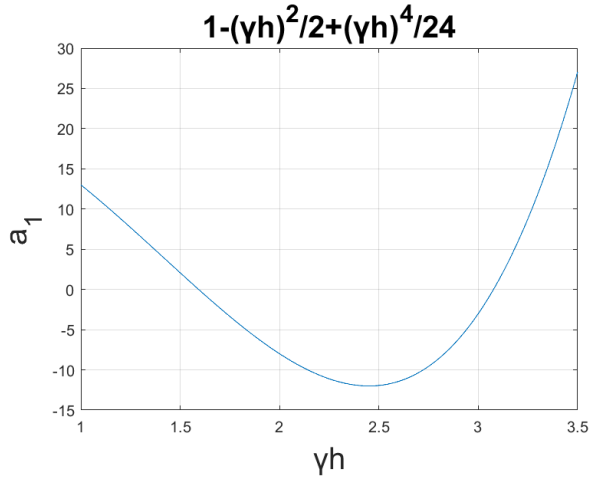

Fig. 5. Function plot of a_1.

The time evolution of system (20) and system (26) depicts at Fig. 6 prove that the two systems are equivalent. Because systems (20) and (26) present the same dynamic, we will adopt system (26) to design the digital FM circuit since it is discrete time system that easily be with the VHDL language. In contrast, system (20) which is a continuous time system.

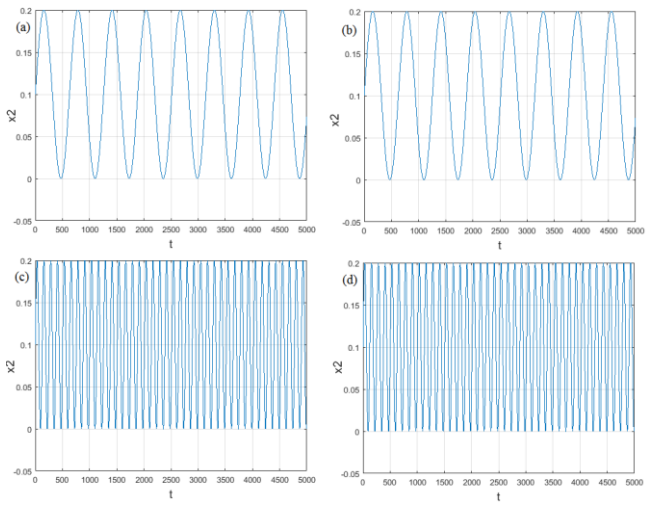

Figure 6: Time evolution of the state variable x_2 of system (20) and system (26): (a) system (20) with $\gamma h = 0.01$; (b) system (26) with $\gamma h = 0.01$; (c) system (20) with $\gamma h = 0.05$; (d) system (26) with $\gamma h = 0.05$

The discretized state variables given in system (26) are implemented using direct VHDL description into Quartus Prime 22.1 design software with a 32 bits floating point of the IEEE754 standards for calculations for the hardware implementation. The dynamic state variables of each sample are sent out into 16 bits sign-fixed point, and the behavioral simulation is done using ModelSim-Altera 6.5e. The Altera chip of type Cyclone IV E EP4CE115F29C7N is the target device. The Register Transfer Level (RTL) schematic presented in Fig. 7 is the top-model of the implemented system (26). Table 1 summarizes some important data after synthesis of the system into Cyclone IV E chip.

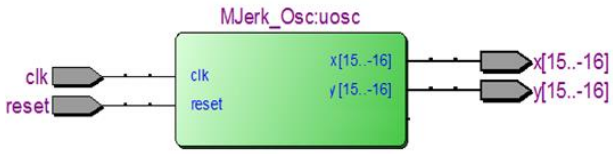

Fig. 7. RTL schematic of system (26).

Table I: Resource Utilizations of Post-Synthesis of System.[26]

Resources	Utilization	Available	Percentage (%)
Logic elements	10 688	114 480	9
Total registers	96	114 480	<1
Memory bits	0	3 981 312	0
Embedded multiplier	35	532	7
Power (mW)	152.83	-	-

The behavioral simulation of system (26) is performed with ModelSim-Altera 6.5e into Quartus Prime 22.1 and presented in Fig. 8.

With the successful simulation of the proposed system, the next step is to implement the digital FM modulator with the parameter γh of the discrete system (26) taken as the input variable where the digital message is to be connected.

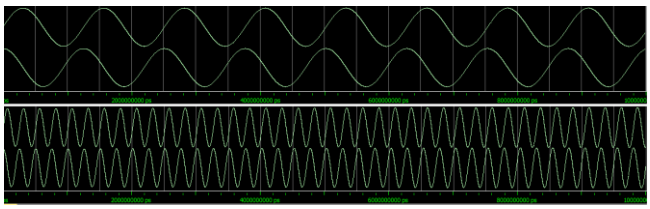

Fig. 8: Simulation result of x, y outputs of system (26) with $\gamma h = 0.05$ and $\gamma h = 0.01$ respectively.

Consequently, a signal generator is design to produce a triangular digital message is to be connected to the modulator as shown in Fig. 9.

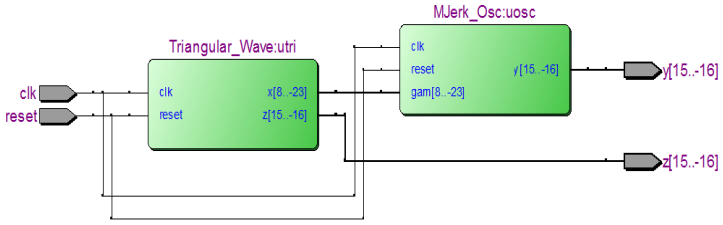

Fig. 9: RTL schematic of the proposed digital FM modulator.

The simulation results presented in Figure 10 show that that the frequency of the y output signal varies in function of the amplitude of the triangular waveform.

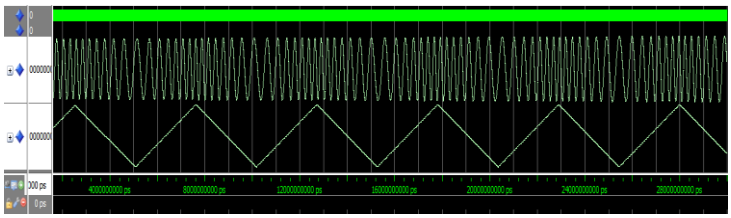

Fig. 10: Simulation results of the FM signal (y) and the triangular message (z).

An FPGA-based implementation is done following the set-up presented in Fig. 11, demonstrating that the proposed digital FM modulator can be implemented practically. The digital output FM signal and the digital triangular wave message signal are present in the audio out of the DE2 115 FPGA board. These signals are produced by audio CODEC fund on the board from digital signals generated by the proposed modulator. The CODEC is used as digital-to-analog converter (DAC).

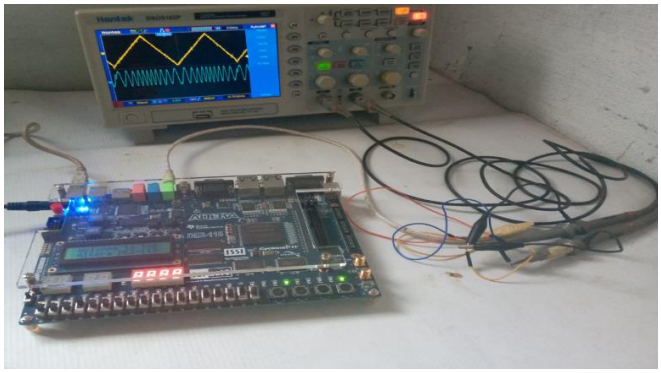

Fig. 11: Experimental set-up of the FPGA implementation of the proposed digital FM modulator using a DE2 115board and the audio CODEC fund on the board as DAC.

The probe of the oscilloscope picks the available signals at the audio out to portray the time evolution of the x and y signals of the modified Jerk oscillator, the message (the triangular signal), and the modulated signal. Setting the initial conditions and parameters used in the

numerical simulation with accuracy, the experimental time evolution of the message and the modulated signals are depicted (Fig. 12). One can see the results obtained from the practical implementation agree with the numerical simulations. It is worth precise that the initial conditions used in numerical simulations and experimental implementation are the same.

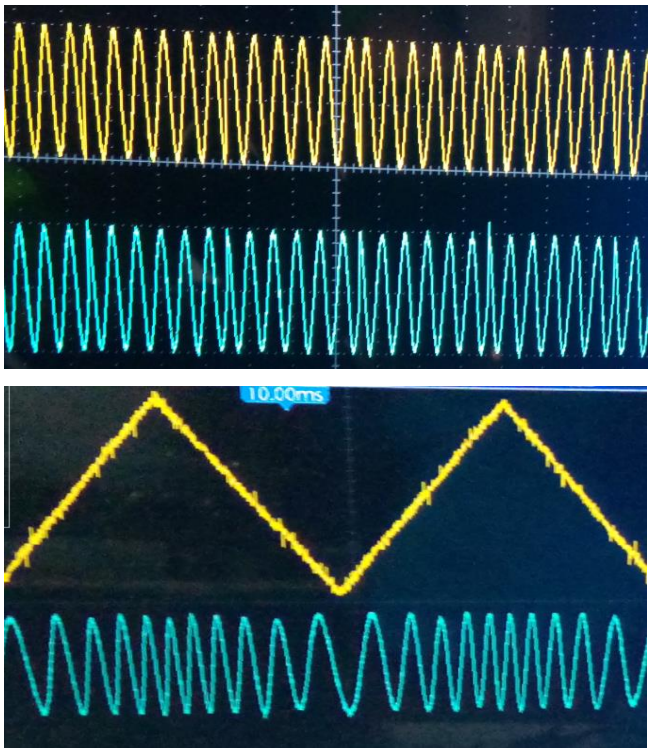

Fig. 12: Experimental time evolution of x and y (top), the message, and the FM signal (down).

5. CONCLUSION

From a modified Jerk circuit, a digital FM modulator has been proposed in this paper. The proposed FM modulator is designed to meet the constraint for software-defined radio and personal wireless communication applications. An FPGA implementation of the proposed digital FM modulator is successfully performed on the targeted device cyclone IV E EP4CE115F29C7N of the FPGA board DE2 115. The numerical and experimental results both show a good agreement. The major result of this work is the implementation of a digital FM modulator using a digital solver circuit. The proposed modulator uses one calculator, which makes it less complex in terms of implementation and has a good performance in terms of resource utilization and power consumption.

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Author contribution statement

Tchahou Tchendjeu Achille Ecladore proposed the model, did the numerical simulation and performed the FPGA implementation. Alombad Henry Njimboh and Noula Mougang Thomas participated in the data analysis at different stages and experimentation. Tchitnga Robert and Fotsin Hillaire Bertrand participated in the data analysis at different stages. All authors revised the manuscript and approved this version.

Declaration of interests

The authors declare that they have no conflict of interest.

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